IDEC Chip Design Contest

A Framed Pulse Width Modulation Transceiver with Low Supply Voltage

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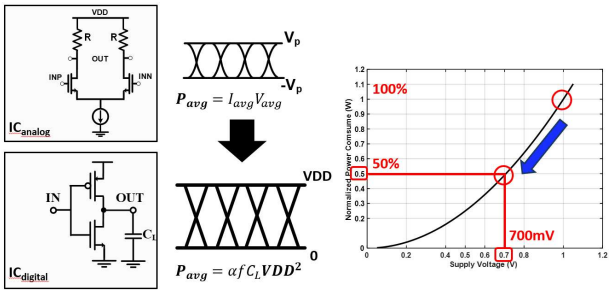
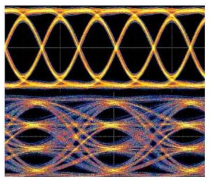
Power Reduction Approach

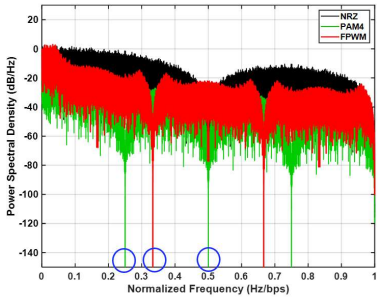
- Low Power Vs. High-Speed Transceiver
  - ✓ Digital Circuitry
  - ✓ Low Supply



- Speed & Power Trade off
- Low VDD limits BW_{IC}

Pulse Amplitude Modulation4 (PAM4)


<Eye Diagram of NRZ & PAM4>

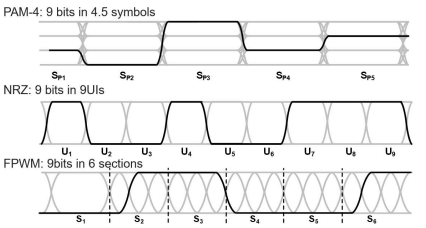


Modulation for Data rate A	PAM2 (NRZ)	PAM4
Symbol rate (Baud)	A	A/2
Bandwidth (Hz)	A/2	A/4
Spectral efficiency	1	2

- Widely used, but based on analog circuits with more power
- Suitable Spectral Efficient Modulation is needed

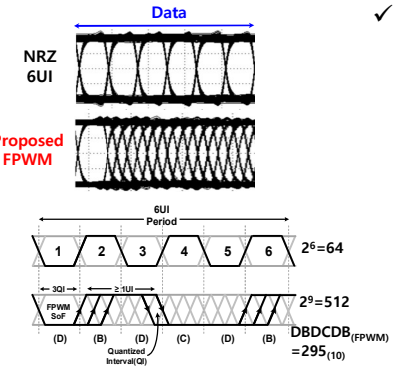
Framed Pulse-width Modulation (FPWM) Transceiver

✓ Time-Domain Modulation



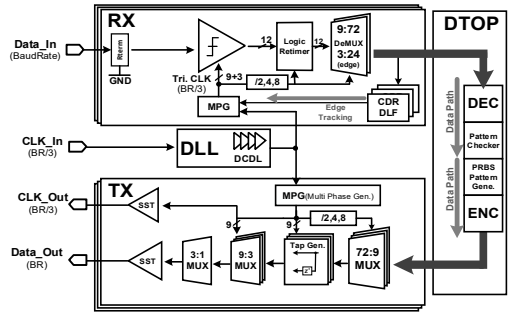
Signaling	Throughput	Nyquist Freq.	Min. Pulse-width
NRZ	*DataRate(DR)*	f_0	T_0
PAM-4	*2DR*	$0.5f_0$	$2T_0$
FPWM	*1.5DR*	$0.67f_0$	$1.5T_0$

- Rail-to-Rail based Modulation
  : Digitally Implementation
- Power reduction w/ Low supply



$$Coding\ Gain = \frac{Data\ Rate}{Baud\ Rate} = \frac{9\ bits}{6\ UIs} = 150\%$$

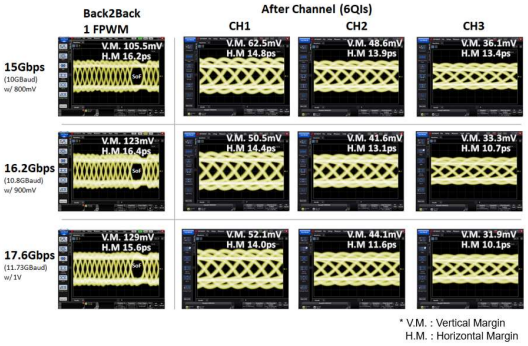
✓ Transceiver Architecture



- 15Gbps(10GBaud) w/ 800mV
- Embedded PRBS Gen./Checker & Enc./Dec.
- DES in Rx & SER in Tx w/ 1-tap FFE
- SAMSUNG 28nm LP Process

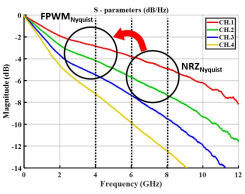
Measurement Result & Die photo

✓ FPWM Eye Diagram

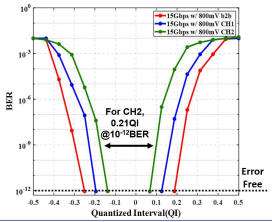


* V.M. : Vertical Margin
H.M. : Horizontal Margin

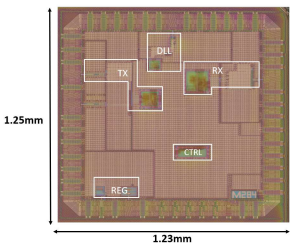
✓ Channel S_{21} Parameter



✓ BER Bathtub Curve



✓ Microphotograph & Effective Area



Block	Area(mm²)	Power(mW)
Tx	0.047	9.18
Rx	0.0461	8.24
DLL	0.0136	5.7
DTOP	0.02	0.8
Overall Blocks	0.1067	23.92

✓ Results

- FoM: 1.59 pJ/bit for 15Gbps/lane
- Area Effective Digital circuit
- Spectral Efficient FPWM mediates BW limits

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